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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/846,146	04/30/2001	Jay A. Kuhn	0325.00452	6032
21363	7590	07/02/2004	EXAMINER	
CHRISTOPHER P. MAIORANA, P.C. 24840 HARPER ST. CLAIR SHORES, MI 48080			PERILLA, JASON M	
			ART UNIT	PAPER NUMBER
			2634	2

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/846,146	KUHN, JAY A.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 30 April 2001.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 15-17 is/are allowed.
 6) Claim(s) 1,5,6,8,9,13 and 14 is/are rejected.
 7) Claim(s) 2-4,7 and 10-12 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 30 April 2001 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-17 are pending in the instant application.

Drawings

2. This application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.
3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feedback of the output signal **hardwired to the first circuit** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 1 is objected to because the claim includes limitations which have no basis in the specification and drawings. The claim recites (with emphasis):

An apparatus comprising: a first circuit configured to (i) select one of a plurality of input signals and (ii) generate (a) an output signal having a frequency and (b) one or more control signals ***in response to a skew signal;*** and a second circuit configured to generate said skew signal in response to said one or more control signals, wherein said first circuit is configured to minimize skew between said selected input signal and a feedback of said output signal in response to said skew signal.

While the generation of an output signal having a frequency may be considered to be responsive to the skew signal, the control signals generated can not according to the present disclosure of the instant application. The skew signal has no impact on the generation of the one or more control signals. Appropriate correction of the claim is required.

5. Claim 14 is objected to because the claim includes limitations which have no basis in the specification and drawings. The claim recites (with emphasis):

An apparatus comprising: means for (i) generating (a) an output signal having a frequency and (b) one or more control signals ***in response to a skew signal*** and (ii) selecting one of a plurality of input signals; means for generating said skew signal in response to said one or more control signals; and means for minimizing timing skew between said selected input signal and a feedback of said output signal.

While the generation of an output signal having a frequency may be considered to be responsive to the skew signal, the control signals generated can not according to the present disclosure of the instant application. The skew signal has no impact on the generation of the one or more control signals. Appropriate correction of the claim is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 9 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while enabling feedback provided after a phase locked loop output, does not reasonably provide enablement for feedback generated without the essential phase locked loop component. The specification including the pending amendment to the drawings does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention commensurate in scope with these claims. Because the first claim includes the limitation of "**a feedback of the output signal**" the specification does not enable the circuit to be implemented external to an existing PLL. The PLL is indeed a necessary in-line component of the apparatus because the preferred embodiment provides both the output signal as well as *the feedback* of the output signal from the PLL. The preferred embodiment is not understood to have feedback directly from the delay line. Therefore, the apparatus according to claim 1 may not be implemented externally to an existing PLL, and claim 9 is thereby not enabled.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 5, 6, 8, 13, and 14 rejected under 35 U.S.C. 102(b) as being anticipated by Yeung et al (US 5889436; hereafter "Yeung").

Regarding claim 1, Yeung discloses by figure 3 an apparatus comprising: a first circuit (refs. 64, 69-72, 80, 40, 20, 79, and 82) configured to (i) select one of a plurality of input signals (outputs of 69-72) by the multiplexer (80) and (ii) generate (a) an output signal ("fout" output from VCO) having a frequency (inherent) and (b) one or more control signals (signal 59 - output of 72); and a second circuit (56) configured to generate a skew signal (62) in response to said one or more control signals (59), wherein said first circuit is configured to minimize skew between said selected input signal (output of multiplexer 80) and a feedback of said output signal in response to said skew signal. The first circuit is configured to minimize skew between said selected input signal and a feedback signal because a portion of the first circuit is a phase locked loop (PLL) which is designed for the purpose of minimizing skew between the output signal fout and a feedback signal of fout fed into the phase detector (20) of the PLL.

Regarding claim 5, Yeung discloses the limitations of claim 1 as applied above. Further, Yeung discloses that the first circuit further comprises a phase locked loop configured to generate said output signal (fig. 3, refs. 40, 20, 79, and "VCO").

Regarding claim 6, Yeung discloses the limitations of claim 1 as applied above. Further, Yeung discloses that the selected input signal comprises a reference clock signal (fig. 3, ref. "fin=19.68Mhz"). The input frequency fin is a reference frequency and it directly results in the generation all of the plurality of input signals.

Regarding claim 8, Yeung discloses the limitations of claim 1 as applied above. Further, Yeung discloses a digitally based skew and low frequency phase noise reduction circuit. It is inherent that the PLL circuit of Yeung performs the operations of

digitally based skew reduction between the input reference frequency and the output signal as well as low frequency phase noise reduction because the purpose of the PLL is to digital skew reduction and low frequency phase noise reduction. It inherently performs both operations because it works to perform digital phase locking.

Regarding claim 13, Yeung discloses the limitations of claim 1 as applied above. Further, Yeung discloses that said one of said input signals (output of any one of 69-72 in figure 3) is hardwired to said first circuit and said output signal is hardwired to said first circuit. The output signal of said first circuit is hardwired to said first circuit because it is generated by said first circuit and is therefore hardwired to it.

Regarding claim 14, Yeung discloses by figure 3 an apparatus comprising: means (refs. 64, 69-72, 80, 40, 20, 79, and 82) for (i) generating (a) an output signal (“fout” output from VCO) having a frequency and (b) one or more control signals (signal 59 - output of 72) and (ii) selecting one of a plurality of input signals (outputs of 69-72) by the multiplexer (80); means (56) for generating a skew signal (62) in response to said one or more control signals (59); and means for minimizing timing skew between said selected input signal and a feedback of said output signal. The PLL means is configured to minimize skew between said selected input signal and a feedback signal because the purpose of the PLL is to minimize skew between the output signal fout and a feedback signal of fout fed into the phase detector (20) of the PLL.

Allowable Subject Matter

9. Claims 2-4, 7, and 9-12 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
10. Indication of allowable subject matter is given regarding claims 15-17.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art not relied upon above is cited to further show the state of the art with respect to skew reducing phase locked loops.

U.S. Pat. No. 6671341 to Kinget et al.

U.S. Pat. No. 5974105 to Wang et al.

U.S. Pat. No. 5838179 to Schmidt.

U.S. Pat. No. 5081655 to Long.

U.S. Pat. No. 6150855 to Marbot.

U.S. Pat. No. 4617679 to Brooks.

U.S. Pat. No. 4755704 to Flora et al.

U.S. Pat. No. 6178123 to Kato et al.

U.S. Pat. No. 6100736 to Wu et al.

U.S. Pat. No. 5771264 to Lane.

U.S. Pat. No. 5463337 to Leonowich.

U.S. Pat. No. 5049766 to van Driest et al.

U.S. Pat. No. 6687320 to Chiu et al.

U.S. Pat. No. 5446867 to Young et al.

U.S. Pat. No. 6201424 to Harrison.

U.S. Pat. No. 6201448 to Tam et al.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (703) 305-0374. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (703) 305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jason M. Perilla
June 21, 2004

jmp



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